## JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD <br> II.B.TECH - I SEMESTER REGULAR EXAMINATIONS NOVEMBER, 2009 <br> DIGITAL LOGIC DESIGN <br> (Common to CSE, IT, CSS)

Time: 3hours
Max.Marks:80

## Answer any FIVE questions

## All questions carry equal marks

1. a) Convert the following to require form
i) $(163.789)_{10}=(\quad)_{8}$
ii) $(101101110001.00101)_{2}=(\quad)_{8}$
iii) $(292)_{16}=(\quad)_{2}$
b) Find the difference of ( $3250-72546)_{10}$ by using 10 's complement.
c) What is meant by self complementing codes.
2. a) Obtain the minimal sum of product expression of given function by using consensus theorem.

$$
f=A \bar{B} \bar{C}+\bar{A} B C+B C D+\bar{A} \bar{C} \bar{D}
$$

b) Which of the following statements are true? Justify.
i) If $\mathrm{A}+\mathrm{B}+\mathrm{C}=\mathrm{C}+\mathrm{D}$ then $\mathrm{A}+\mathrm{B}=\mathrm{D}$
ii) If $\mathrm{A}+\mathrm{B}=\mathrm{C}$ then $A \bar{D}+B \bar{D}=C \bar{D}$
3. a) Design a circuit which finds the 2 'S complement of a 4 bit binary number. Write HDL program for this design.
b) Prove that NAND and NOR operations are commutative but not Associative.
4. a) Design a BCD to Gray code converter using 8:1 MUXS.
b) Write a HDL program to model an 8 bit comparator using 2 bit comparators. [8+8]
5. a) Draw a neat circuit diagram of positive triggered D flip flop and explain its operation.
b) Design a master slave JK flip flop by writing HDL program to describe the flip flop.
6. a) Design a 4 bit Ripple counter using T flip flop. Explain using wave forms.
b) Write HDL program in behaviour model to design a 4 bit shift left register. [8+8]
7. a) Design a Hamming code encode to obtain 11 bit code from the circuit use PLAS. b) Write a brief note ion ROMS.
8. a) Design an asynchronous sequential circuit with the following excitation requirement and output functions

$$
\begin{align*}
& \quad Y_{1}=x_{1} x_{2}+x_{1} \overline{y_{2}}+\overline{x_{2}} y_{1} \\
& Y_{2}=x_{2}+x_{1} \overline{y_{1}} y_{2}+\overline{x_{1}} y_{1} \\
& Z=x_{2}+y_{1} \tag{8+8}
\end{align*}
$$

b) Design a hazard tree circuit to implement $\mathrm{y}=\left(x_{1}+x_{2}\right)\left(x_{2}+x_{3}\right)$

