Code No: RR320501 **Set No. 1**

III B.Tech II Semester Regular Examinations, Apr/May 2007
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. What is meant by parallelism in uniprocessor systems? Identify the various mechanisms that have been developed for this purpose and describe them. [16]
2. (a) Describe the various issues and design principles of pipelines instruction units.
   (b) What are carry − save adders? Design a pipeline multiplication scheme using the carry-save adders. [8+8]
3. Discuss the Mesh-connected Illiac Network with a neat diagram and give its routing functions and importance. [16]
4. Discuss sorting patterns with respect to three ways of indexing the$PE's$. [16]
5. Explain various algorithms for Bus arbitration in multiprocessor organization.[16]
6. (a) Discuss different problems associated with multi cache and suggest suitable solutions.
   (b) Classify various multiprocessor operating systems. Briefly, give their features. [8+8]
7. (a) Explain the organization of a dynamic data flow computer.
   (b) What is data flow graph? Explain how a data flow graph constructed. [8+8]
8. (a) Explain the functions of bus in C.mmp
   (b) Describe two stage memory configuration in C.mmp. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR320501 **Set No. 2**

III B.Tech II Semester Regular Examinations, Apr/May 2007
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Draw the structure of a parallel memory system with consecutive words in a module and describe its working. Also highlight its merits and demerits.
   (b) Draw the structure of a parallel memory system with consecutive words in consecutive modules and describe its working. Also highlight its merits and demerits. [8+8]
2. Explain different vector Processing methods with suitable illustrations. [16]
3. (a) What functional switch boxes and control mechanisms are used in constructing multistage cube networks.
   (b) Explain the network topology used in STARAN Flip Network. [8+8]
4. (a) Explain the implementation of SIMD fast Fourier Transform.
   (b) Explain on the connection issues in while using SIMD inter connection networks. [8+8]
5. (a) Explain the operation of a multiprocessor system with multiport memory.
   (b) The multistage networks are modular and easy to control. Justify this. [10+6]
6. (a) Define the term nonpreemptive scheduling. With an example illustrate the Hu's optimal algorithm.
   (b) Explain briefly a simple queueing model for multiprocessor scheduling.[10+6]
7. (a) Describe any four systolic array configurations.
   (b) Describe how algorithms are mapped into VLSI arrays. [8+8]
8. (a) Discuss about a simple queuing structure with a single processor having inter arrival time and service times.
   (b) Discuss in detail the performance of M/M/n queuing structure. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR320501 **Set No. 3**

III B.Tech II Semester Regular Examinations, Apr/May 2007
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What is the degree of parallelism? Explain the classification of computer systems based on Handlers Classification.
   (b) Explain parallelism and pipelining.Describe a computer classification based on these concepts. [8+8]
2. (a) Differentiate between linear and nonlinear piplines. Give their sample pipeline structures and reservation tables.
   (b) Explain internal forwarding techniques with examples. What are its advantages? [8+8]
3. Explain Cube Interconnection Network with 8 nodes and give its routing functions. [16]
4. Write an algorithm that performs an SIMD matrix multiplication with a time complexity of order o(n^2), Give its memory allocation of the algorithm. [16]
5. (a) Describe a multiport memory with private memories.
   (b) Discuss how 1-by-8 demultipluxer is derived from 2x2 switches.
   (c) Give the circual diagram of a Buffered 2x2 crossbar. [8+4+4]
6. (a) Write an asynchronous parallel algorithm for finding the zeros of a function f(x) using Newton's iteration method.
   (b) Explain briefly the methodology for evaluating the performance of a parallel algorithm. [8+8]
7. (a) Compare data driven and dependence driven computing models.
   (b) Explain the multilevel program abstraction in the event driven data flow computing model. [8+8]
8. (a) Explain the staging memory concept in MPP and instruction set of the MPP.
   (b) How new image processing techniques are developed using MPP. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR320501 **Set No. 4**

III B.Tech II Semester Regular Examinations, Apr/May 2007
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What are the different types of memories that are present in a memory hierarchy? Describe the characteristics of each of these memories.
   (b) What is meant by interleaving memory addresses? Describe the different ways of implementing interleaving schemes. Illustrate with the help of proper diagrams. What are the relative merits and demerits of these schemes? [8+8]
2. (a) What is collision ? Explain different ways if its prevention.
   (b) What is memory hierarchy ? How memory hierarchy improves the performance of a single processor system. [8+8]
3. Explain the working of a Barrel Shifter with 16 nodes and give its routing functions. [16]
4. (a) What is an associative memory? Discuss a simple associative memory organization with suitable diagrams.
   (b) Explain the architecture of PEPE association processor. [8+8]
5. (a) Describe the desirable architectural features for a processor to be effective in a multiprocessing system.
   (b) Explain the architecture of Honeywell 60/66 multiprocessor system. [8+8]
6. (a) List the major characteristics, advantages and shortcomings of three types of multiprocessor operating systems.
   (b) List the four main sources of performance degradation of the dynamic coherence check algorithm. [12+4]
7. (a) Explain the VLSI arithmetic module for the multiplication of the sequences of 2 x 2 matrices.
   (b) Explain the principles of a pipelined VLSI matrix inverter. [8+8]
8. (a) How memory mapping is done in Cyber-205? Explain
   (b) List various functions of virtual memory in Cyber 205.
   (c) Describe any two special vector instruction of Cyber 205. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆