[4+4+4+4]

III B.Tech I Semester Regular Examinations, November 2007 COMPUTER ORGANISATION (Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Control Engineering and Electronics & Telematics) Time: 3 hours Max Marks: 80 Answer any FIVE Questions All Questions carry equal marks

- 1. (a) Discuss about Flynn's classification of computers.
 - (b) Explain about communication topologies used in multiprocessors. [16]
- 2. Write about direct, indirect, register direct, register indirect, immediate, implicit, relative, index, and base address mode of addressing. Why do we need so many addressing modes? Is the instruction size influenced by the number of addressing modes which a processor supports? State whether the number of addressing modes will be more in RISC or CISC? [16]
- 3. (a) Why do we need subroutine register in a control unit? Explain. [8]
 - (b) Explain nanoinstructions and nanometry. Why do we them? [8]
- 4. Explain the computational errors. Why do they occur?. Give some problems where these errors are catastrophic. Also, give some practical examples (algorithms) where error gets
 - (a) accumulated and(b) multiplies. [16]
- 5. Explain the following with applications for each:
 - (a) ROM
 - (b) PROM
 - (c) EPROM
 - (d) EEPROM.
- 6. Explain the following:
 - (a) Isolated Vs Memory mapped I/O
 - (b) I/O Bus Vs Memory Bus
 - (c) I/O Interface
- (d) Peripheral Devices. [4+4+4]
 7. (a) What is pipelining? Explain. [8]
 - (b) Explain four segment pipelining. [8]

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- 8. (a) Explain multiport memory organization with a neat sketch.
 - (b) Explain system bus structure for multiprocessors with a neat sketch. [8+8]

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- 1. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous. [10]
 - (b) Distinguish between high level and low level languages? What are the requirements for a good programming language? [6]
- 2. Design register selection circuit to select one of the four 4-bit registers content on to bus. Give fuller explanation. [16]
- 3. (a) How do we reduce number of microinstructions. What are micro-subroutines? [8]
 - (b) Explain nanoinstructions and nanometry. Why do we need them? [8]
- 4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
 - (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. [8]
- 5. (a) What is the functioning of a Flash Memory? Explain. [8]
 - (b) Give the detailed picture of Memory Hierarchy. [8]
- 6. Explain the following:
 - (a) Asynchronous Serial Transfer
 - (b) Asynchronous Communication Interface. [8+8]
- 7. Explain three segment instruction pipeline. Show the timing diagram and show the timing diagram with data conflict. [16]
- 8. (a) Explain the working of 8 x 8 Omega Switching network.
 - (b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch. [8+8]

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1.	Dist by o calcu and	inguish between error detection and correction codes. What do you uno odd parity and even parity?. What is odd function and even functi- ulate odd and even parity values which functions can be used? Calcul even parity values for all hexadecimal digits 0-9 and A-F.	lerstand on?. To ate Odd [16]
2.	(a)	Explain about stack organization used in processors. What do you une by register stack and memory stack?	derstand [10]
	(b)	Explain how $X=(A+B)/(A-B)$ is evaluated in a stack based compute	er. [6]
3.	(a)	How do you map micro-operation to a micro instruction address.	[8]
	(b)	Hardwired control unit is faster than microprogammed control unit. this statement.	Justify [8]
4.	(a)	What is the use of fast multiplication circuits? Write about array mu	ltipliers. [8]
	(b)	Multiply 10111 with 10011 using booths algorithm.	[8]
5.	(a)	Explain how the Bit Cells are organized in a Memory Chip.	[8]
	(b)	Explain the organization of a 1K x 1 Memory with a neat sketch.	[8]
6.	(a)	What is Direct Memory Access? Explain the working of DMA.	
	(b)	What are the different kinds of DMA transfers? Explain.	
	(c)	What are the advantages of using DMA transfers?	[8+4+4]
7.	(a)	What is pipeline? Explain.	[8]
	(b)	Explain arithmetic pipeline.	[8]
8.	(a)	Explain the working of 8 x 8 Omega Switching network.	

(b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch. [8+8]

- (b) Explain about daisy chain based bus arbitration. [16]
- 2. (a) Design a circuit transferring data from a 4bit register which uses D flip-flops to another register which employs RS flip-flops. [8]
 - (b) What are register transfer logic languages? Explain few RTL statement for branching with their actual functioning. [8]
- 3. (a) Support the statement Instruction Set Architecture has impact on the processors microarchitecture. [8]
 - (b) How do we reduce number of microinstructions? What are micro-subroutines? [8]
- 4. (a) Draw a flow chart which explains multiplication of two signed magnitude fixed point numbers. [8]
 - (b) Multiply 10111 with 10011 with the above procedure given (a). Show all the registers content for each step. [8]
- 5. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. [16]
- 6. (a) What is polling? Explain in detail.
 (b) What is daisy chaining? Explain.
 7. (a) What is pipeline? Explain space-time diagram for Pipeline.
 (b) Explain pipeline for floating point addition and subtraction.
- 8. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those. [6]
 - (b) Explain time-shared common bus Organization. [5]
 - (c) Explain system bus structure for multiprocessors. [5]