Code No: R05310201 **Set No. 1**

III B.Tech I Semester Supplimentary Examinations, February 2008
COMPUTER ORGANISATION
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering, Electronics & Control Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about sign magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable.
   (b) Give means to identify whether or not an overflow has occurred in 2s complement addition or subtraction operations. Take one example for each possible situation and explain. Assume 4 bit registers.
   (c) Distinguish between tightly coupled microprocessors and tightly coupled Microprocessors. [16]
2. (a) Explain about stack organization used in processors. What do you understand by register stack and memory stack? [10]
   (b) Explain how X=(A+B)/(A-B) is evaluated in a stack based computer. [6]
3. (a) Support or oppose the statement. The control unit is a firmware? [8]
   (b) Support or oppose the statement. If we want to add a new machine language instruction to a processors instruction set, simply write a C program and compile and store the resultant code in control memory. [8]
4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
   (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. [8]
5. (a) Explain how the Bit Cells are organized in a Memory Chip. [8]
   (b) Explain the organization of a 1K x 1 Memory with a neat sketch. [8]
6. What are the different kinds of I/O Communication techniques? What are the relative advantages and disadvantages? Compare and contrast all techniques. [16]
7. Explain the following with related to the Instruction Pipeline
   (a) Pipeline conflicts
   (b) Data dependency
   (c) Hardware interlocks
   (d) Operand forwarding
   (e) Delayed load

(f) Pre-fetch target instruction

(g) Branch target buffer

(h) Delayed branch. [8×2=16]

8. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those. [6]

(b) Explain time-shared common bus Organization. [5]

(c) Explain system bus structure for multiprocessors. [5]

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Code No: R05310201 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the terms computer architecture, computer organization and computer design in a detailed fashion. [8]
   (b) Explain about MIPS, FLOPS rating of a processor. How do we arrive at these values. [8]
2. (a) What is the use of buffers. Explain about tri-state buffers. Explain about high impedance state. [6]
   (b) Explain commonly employed bit shift operators such as shift left, right, circular shift left/right and arithmetic shift left/right. Assume an 8-bit register, give an example for each [10]
3. (a) Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction. [8]
   (b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. [8]
4. Draw a flowchart to explain how two IEEE 754 floating point numbers can be added, subtracted and multiplied. Assume single precision numbers. Give example for each [16]
5. (a) "In paged segmentation, the reference time increases and fragmentation decreases", Justify your answer.
   (b) A Virtual Memory System has an address space of 8K words and a Memory space of 4K words and page and block sizes of 1K words. Determine the number of page faults for the following page replacement algorithms: 1) FIFO 2) LRU if the reference string is as follows: 4,2,0,1,2,6,1,4,0,1,0,2,3,5,7. [8+8]
6. (a) Explain bit oriented and character oriented protocols in serial communication.
   (b) What are the different issues behind serial communication? Explain. [8+8]
7. (a) What is pipeline? Explain. [8]
   (b) Explain arithmetic pipeline. [8]
8. What is cache coherence and why is it important in shared memory multiprocessor systems? How can the problem be solved with a snoopy cache controller? [16]

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Code No: R05310201 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous. [10]
   (b) Distinguish between high level and low level languages? What are the requirements for a good programming language? [6]
2. Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic. [16]
3. (a) Differentiate between microprogramming and nanoprogramming. [8]
   (b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. [8]
4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
   (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. [8]
5. Compare and contrast Asynchronous DRAM and Synchronous DRAM. [16]
6. What are the different kinds of I/O Communication techniques? What are the relative advantages and disadvantages? Compare and contrast all techniques. [16]
7. Explain the following with related to the Instruction Pipeline
   (a) Pipeline conflicts
   (b) Data dependency
   (c) Hardware interlocks
   (d) Operand forwarding
   (e) Delayed load
   (f) Pre-fetch target instruction
   (g) Branch target buffer
   (h) Delayed branch. [8×2=16]
8. (a) Explain the working of 8 x 8 Omega Switching network.

(b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch. [8+8]

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Code No: R05310201 **Set No. 4**

III B.Tech I Semester Supplimentary Examinations, February 2008
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about sign magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable.
   (b) Give means to identify whether or not an overflow has occurred in 2s complement addition or subtraction operations. Take one example for each possible situation and explain. Assume 4 bit registers.
   (c) Distinguish between tightly coupled microprocessors and tightly coupled Microprocessors. [16]
2. . Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic. [16]
3. (a) Support the statement Instruction Set Architecture has impact on the processors microarchitecture. [8]
   (b) How do we reduce number of microinstructions? What are micro-subroutines? [8]
4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
   (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. [8]
5. Compare and contrast Asynchronous DRAM and Synchronous DRAM. [16]
6. (a) What are the different types of I/O communication techniques? Give brief notes.
   (b) In the above techniques, which is the most efficient? Justify your answer.[8+8]
7. (a) What is meant by arithmetic pipeline? Explain.
   (b) Explain pipeline for floating point addition and subtraction. [8+8]
8. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those. [6]
   (b) Explain time-shared common bus Organization. [5]
   (c) Explain system bus structure for multiprocessors. [5]

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