KAKATIYA UNIVERSITY: WARANGAL

TIME TABLE M.TECH I Year II SEMESTER EXAMINATION

CENTRE: Chaitanya Institute of Technology & Science, Kishanpura, HNK, Wgl.

a) Kakatiya Institute of Technology and Science, Warangal b) Warangal Institute of Technology & Science, Oorugonda, Warangal
c) Chaitanya Institute of Technology & Science, Kishanpura, HNK, Wgl. d) Vinuthna Institute of Technology & Science, Hasanparthy
e) KU College of Engineering & Technology, KU Campus

TIME:: 02.00 pm to 05.00 pm

Date & Day	Structural & Construction Engineering	Design Engineering	CAD/CAM	Digital Communication	Software Engineering	Computer Science and Engineering	VLSI & Embedded System Design	VLSI Systems Design	Power Electronics
15-12-2015 Tuesday	Theory of Elasticity and Plasticity	+Finite Element Analysis	+Finite Element Analysis	Coding Theory	Advanced DBMS	Java & Web Technology	Mixed Signal Design	Hardware software Co Design	Power Electronic Control of AC Drives
17-12-2015 Thursday	Design of Bridges	Advanced Mechanism Design & analysis	Computer Integrated Manufacturing	Communication System Modeling	Information Systems & Auditing	Advanced Data Mining	@VLSI Physical Design	@VLSI Physical Design	Microprocessor and Microcontroller
19-12-2015 Saturday	Seismic Analysis of Structures	-Advanced Materials Science and Engineering	-Advanced Materials Science and Engineering	Multimedia Communications & System Design	Real Time Systems	Soft Computing	Embedded System Modeling, Synthesis and Verification	Digital Image Processing	Flexible AC Transmission Systems (FACTS)
23-12-2015 Wednesday	Construction Planning and Management	*Automation & Robotics	*Automation & Robotics	Digital Image Processing	Software Architecture	Software Quality Assurance & Testing	$Low power VLSI Design	$Low power VLSI Design	Neural and Fuzzy Systems
28-12-2015 Monday	Personal Management	MEMS & Nano Technology	Production and operations Management	**ELECTIVE – II** a) DSP Processors b) Satelite Communication c)Radar Signal Processing	Software Quality Assurance & Testing	**ELECTIVE – II** b)Object Oriented Analysis and Design	0Design for Testability	0Design for Testability	**ELECTIVE – III** Power Quality
31-12-2015 Thursday	**ELECTIVE –II** b) Design of special Structures c) Legal Issues in Construction d) Financial Management	**ELECTIVE – II** a) Fault Diagnosis of Machines	**ELECTIVE – II** c) Flexible manufacturing System		**ELECTIVE – II** a) Data Mining & Data Warehousing	**ELECTIVE –III** a) Cloud Computing c)Information Retrival Systems	**ELECTIVE – II** +(b)CPLD & FPGA, Architectures and Applications c) Cellulor and Mobile Communication	**ELECTIVE – II** +(b)CPLD & FPGA, Architectures and Applications	**ELECTIVE – IV** a)Reliability Engineering Embedded Systems c) Embeded Systems

CONTROLLER OF EXAMINATIONS

Note: - *Any Omission or Clash in the Time-Table may kindly be intimated to the Controller of Examination, K.U., Warangal, immediately.*